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In the Claims:

Please amend Claims 1, 6, 7, and 8 and cancel Claim 9 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) Multi-processor computer system comprising at least two processors (1) for parallel execution of processes, at least two cache memory units (2), each being associated with and connected to a separate processor (1) of the at least two processors, a connection bus (4) connecting said processors (1) and said cache memory units (2), and a process list unit (3) connected to said connection ~~line~~ bus (4) for storing a process list of processes to be available for execution by said processors (1), wherein said processors (1) are adapted for loading a global wake-up variable signaling process additions of processes to said process list into their associated cache memory unit (2), for switching into a low-power mode if said process list contains no process for execution by said processors (1) and for switching into a normal-power mode if said wake-up variable signals an addition of a process to said process list.

2. (Original) Multi-processor computer system as claimed in claim 1, wherein said processors (1) are adapted to switch into the normal-power mode if the wake-up variable held in the associated cache memory units (2) is changed due to an addition of a process to said process list.

3. (Original) Multi-processor computer system as claimed in claim 1, wherein said processors (1) are adapted to execute a store command on the wake-up variable when adding a process to said process list.

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4. (Original) Multi-processor computer system as claimed in claim 1, wherein said processors (1) are adapted to send a request to other processors to drop the wake-up variable from their associated cache memory unit when adding a process to said process list.

5. (Original) Multi-processor computer system as claimed in claim 1, wherein said computer system is adapted for implementing an invalidation based cache coherence protocol.

6. (Currently Amended) Processor for use in a multi-processor computer system comprising at least two processors (1) for parallel execution of processes, at least two cache memory units (2), each being associated with and connected to a separate processor (1) of the at least two processors, a connection bus (4) connecting said processors (1) and said cache memory units (2), and a process list unit (3) connected to said connection ~~line~~ bus (4) for storing a process list of processes to be available for execution by said processors (1), wherein ~~said a processor (1)~~ a processor (1) of the at least two processors is adapted for loading a global wake-up variable signaling process additions of processes to said process list into its associated cache memory unit (2), for switching into a low-power mode if said process list contains no process for execution by said processor and for switching into a normal-power mode if said wake-up variable signals an addition of a process to said process list.

7. (Currently Amended) Method of scheduling the execution of processes in a multi-

processor computer system comprising at least two processors (1) for parallel execution of processes, at least two cache memory units (2), each being associated with and connected to a separate processor of the at least two processors (1), a connection bus (4) connecting said processors (1) and said cache memory units (2), and a process list unit (3) connected to said connection ~~line~~ bus (4) for storing a process list of processes to be available for execution by said processors (1), said method comprising the steps of: loading a global wake-up variable signaling process additions of processes to said process list by a processor (1) into its associated cache memory unit (2), adding a process to said process list, and changing the wake-up variable signaling said addition of a process to said process list thus causing said processor (1) to switch from a low-power mode into a normal-power mode.

8. (Currently Amended) Method of executing a process by a processor in a multi-processor computer system comprising at least two processors (1) for parallel execution of processes, at least two cache memory units (2), each being associated with and connected to a separate processor (1) of the at least two processors, a connection bus (4) connecting said processors (1) and said cache memory units (2), and a process list unit (3) connected to said connection ~~line~~ bus (4) for storing a process list of processes to be available for execution by said processors (1), said method comprising the steps of: loading a global wake-up variable signaling process additions of processes to said process list into an associated cache memory unit (2), switching into a low-power mode if said process list contains no process for execution by said processor (1), switching into a normal-power mode if said wake-up variable signals an addition of a process to said process list, and accessing said process list to get said added process for execution.

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9. (Cancelled)